REMARKS

Applicants are in receipt of the Office Action mailed July 29, 2004. Claims 1 – 24 were pending. Applicants have amended claims 1, 5 – 8, 10, and 20 – 24. Applicants have cancelled claim 9. Claims 1 – 8 and 10 – 24 therefore remain pending in the application.

Claims 20 – 24 were rejected under 35 U.S.C. §101 for being directed to non-statutory subject matter. Applicants have amended claims 20 – 24 to overcome this rejection.

Claims 1 – 24 were rejected under 35 U.S.C. §102(e) as being anticipated by Arimilli et al. (USPN 6,480,975, hereinafter "Arimilli"). Applicants respectfully traverse this rejection.

Applicants amended claim 1 recites in pertinent part:

> "...detecting an error in data stored in a directory cache in a system;
> determining if the detected error is correctable; and
> making at least a portion of the directory cache unavailable to one or more resources in the system in response to determining that the error is uncorrectable, **wherein making at least the portion of the directory cache unavailable comprises generating a cache miss in response to a request to access the directory cache.**"

In contrast, Arimilli teaches at col. 6, lines 2 – 14, that "This output is connected to a retry circuit 82 and an ECC circuit 84. Retry circuit 82 causes the cache operation to be repeated after a delay sufficient to allow ECC circuit 84 to complete its operation. ECC circuit 84 uses all of the bits from all address tags in congruence class 74, and further uses bits from a special ECC field 86. Only one ECC field is provided for each congruence class, rather than providing one ECC field for each cache block. When ECC circuit 84 operates on the input values, it generates corrected values which are fed back to the cache blocks and ECC field of the congruence class. *If a double-bit error is detected,*

operation of the processing unit can be halted using an appropriate circuit 88." (Emphasis added)

Arimilli teaches halting operation of the processing unit if a double-bit error is detected, not "**generating a cache miss in response to a request to access the directory cache**," as recited in Applicants' amended claim 1. Accordingly, claim 1, along with its dependent claims 2 – 8, is believed to patentably distinguish over the cited art.

Independent claims 10 and 20 recite similar limitations to claim 1, and are thus also believed to patentably distinguish over the cited art for at least the above reasons.

Furthermore, Applicants can find no teaching or suggestion in Arimilli of a method comprising "**testing the directory cache based on determining that the error is uncorrectable**," as recited in Applicants' amended claim 6. Arimilli teaches a cache which allows for single-bit error correction and double-bit error detection using error correcting codes (col. 4, lines 25 – 26) but does not teach "testing the directory cache based on determining that the error is uncorrectable."

Accordingly, Applicants' claim 6 is believed to further patentably distinguish over the cited art. Claim 16 recites similar limitations, and is thus also believed to patentably distinguish over the cited art.

CONCLUSION

In light of the foregoing remarks, Applicant respectfully submits the application is now in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-55600/BNK.

Respectfully submitted,

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